Amendments to the Claims

In the Claims:

1. (currently amended) A method of fabricating an integrated circuit, comprising the following steps performed in order of:

forming an interlevel dielectric layer over a semiconductor body;

forming an intrametal dielectric layer over said interlevel dielectric layer;

forming a hardmask over said intrametal dielectric layer;

forming a via pattern over said hardmask;

selectively etching a via through said hardmask;

extending said via by selectively etching said intrametal dielectric layer;

depositing a BARC layer over said hardmask and within said via, wherein said BARC layer is significantly thicker within said via than over said hardmask;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and wherein at the conclusion of said etching a trench step said via extends through said interlevel dielectric layer.

2. (original) The method of claim 1, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer; and extending said via by selectively etching through said shelf layer using said via pattern after said etching a via step.

3. (original) The method of claim 2, further comprising the step of extending said via by selectively etching through said interlevel dielectric layer after said step of etching said shelf layer and prior to depositing said BARC layer.

4. (original) Th method of claim 3, wh rein said depositing a BARC layer step fills said via to a level approximately even with a height of said interlevel dielectric.

5. (original) The method of claim 3, further comprising the step of removing a remaining portion of said BARC layer after said etching a trench step.

6. (original) The method of claim 1, further comprising the step of filling said trench and via with copper.

7. (original) The method of claim 1, wherein said intrametal dielectric layer comprises an organic polymer.

8. (original) The method of claim 1, wherein said intrametal dielectric layer and said interlevel dielectric layer comprise SiLK™.

9. (original) The method of claim 1, wherein said interlevel dielectric comprises an organic polymer.

10. (currently amended) A method of fabricating an integrated circuit, comprising the following steps performed in order~~of~~:

forming an interlevel dielectric layer over a semiconductor body;

forming a shelf layer over said interlevel dielectric layer;

forming an intrametal dielectric layer over said shelf layer;

forming a hardmask over said intrametal dielectric layer;

forming a via pattern over said hardmask;

selectively etching a via through said hardmask;

extending said via by selectively etching said intrametal dielectric layer and said shelf layer;

depositing a BARC layer ov r said hardmask and within said via after said extending said via step;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and extends said via through said interlevel dielectric layer.

11. (previously added) A method of fabricating an integrated circuit, comprising the steps of:

forming an interlevel dielectric layer over a semiconductor body;

forming an intrametal dielectric layer over said interlevel dielectric layer;

forming a hardmask over said intrametal dielectric layer;

forming a via pattern over said hardmask;

selectively etching a via through said hardmask;

extending said via by selectively etching said intrametal dielectric layer and said interlevel dielectric layer;

depositing a BARC layer over said hardmask and within said via, after the extending said via step;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

12. (previously added) The method of claim 11, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer; and extending said via by selectively etching through said shelf layer using said via pattern after said etching a via step.

13. (previously added) The method of claim 11, wherein said depositing a BARC layer step fills said via to a level approximately even with a height of said interlevel dielectric.

14. (previously added) Th m thod of claim 11, further comprising the step of removing a remaining portion of said BARC layer after said etching a trench step.